NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
राष्ट्रीय प्रौद्योगिकी संस्थान कर्नाटक, सुरत्कल
P.O SRINIVASNAGAR, MANGALORE - 575025

IrIS

EC Call Letter List

M Tech. (Research), 2025 - 26

The following applicants have been selected for written exam and/or interview for the department for the department of Electronics and Communication Engineering for M Tech. (Research) Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	VISHWAS A SHANBHAG	MTR2025VL0003	VLSI Design
2	Kavya K G	MTR2025VL0007	VLSI Design
3	Shubham Akela	MTR2025VL0008	VLSI Design
4	NAVEEN GURUGUBELLI	MTR2025VL0009	VLSI Design
5	NAVEEN GURUGUBELLI	MTR2025SP0002	Signal Processing and Machine Learning
6	Chiluka Navya	MTR2025VL0010	VLSI Design
7	Nalla Pallavi	MTR2025VL0011	VLSI Design
8	Bhukya Saraswathi	MTR2025SP0003	Signal Processing and Machine Learning
9	AATHARVAA KETAN SHIVESHWARKAR	MTR2025VL0012	VLSI Design
10	Hema naga vaishnavi	MTR2025VL0013	VLSI Design
11	Narayan Pujari	MTR2025VL0014	VLSI Design

EC Call Letter List

M Tech. (Research), 2025 - 26

12	Narayan Pujari	MTR2025SP0004	Signal Processing and Machine Learning
13	BURRA VIJAY KUMAR	MTR2025VL0015	VLSI Design
14	Akash S Sinnoor	MTR2025VL0016	VLSI Design
15	SIBA PRASAD MISHRA	MTR2025VL0017	VLSI Design
16	BITRAGUNTA VENKATA SREE KOUSIK	MTR2025VL0018	VLSI Design
17	Gaargi H Amarendra	MTR2025VL0019	VLSI Design
18	Gaargi H Amarendra	MTR2025SP0005	Signal Processing and Machine Learning
19	S Deepthi Nayak	MTR2025VL0020	VLSI Design
20	Chandan B K	MTR2025VL0021	VLSI Design
21	RAJEEV RANJAN	MTR2025VL0022	VLSI Design
22	Ojas Sharma	MTR2025VL0023	VLSI Design
23	Anas Ahmad	MTR2025SP0008	Signal Processing and Machine Learning
24	Shreyank G Kamalapur	MTR2025VL0024	VLSI Design
25	Shreyank G Kamalapur	MTR2025SP0010	Signal Processing and Machine Learning
26	Shreyank G Kamalapur	MTR2025CN0005	Communication Engineering and Networks

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EC Call Letter List

M Tech. (Research), 2025 - 26

27	Logeshwaran R	MTR2025VL0026	VLSI Design
28	Chandan B K	MTR2025SP0012	Signal Processing and Machine Learning
29	Kartikey Teotia	MTR2025VL0028	VLSI Design
30	Gona Meghana	MTR2025VL0030	VLSI Design
31	ARNOB DAS	MTR2025VL0031	VLSI Design
32	Gona Meghana	MTR2025SP0014	Signal Processing and Machine Learning
33	V SAAI MIRUTHUNJAYAN	MTR2025VL0032	VLSI Design
34	Aritra Das	MTR2025VL0033	VLSI Design
35	SHUBHAM SENWAR	MTR2025SP0015	Signal Processing and Machine Learning

M. Ramesh

May 05, 2025

Head Of Department

Electronics and Communication Engineering

PROF & HEAD
Dept. of Electronics & Communication Engg.
एन.आई.टी.के. सुरत्कल/NITK Surathkal
मंगलूरु / MANGALURU - 575 025

Dean Academics

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA SURATHKAL
P.O. SRINIVASNAGAR, MANGALURU-575 025
Telephone: 0824-2473046, Website: www.ece.nitk.ac.in

Date: 05-05-2025

Syllabus for M. Tech. (Research) Aptitude Test- May 2025

Date and time for:

- **Document verifications:** May 21, 2025, 9:00 AM onwards
- **Written Test:** May 21, 2025, 2:00PM to 3:00PM.
- **Interview**: May 22, 2025, 9:00AM onwards

Question Paper format: It is a common paper for all the three streams offered by Department of Electronics and Communication Engineering. There will be 20 questions and all questions are compulsory. The questions are in the MCQ format.
Marking scheme: Every correct answer: 1 mark, Every wrong answer: -0.25 mark.

Note: Total duration of Exam is one hour. Use of Calculator is permitted.

Linear Algebra, Calculus, Differential and Difference equations. Numerical methods, Transforms, Linear circuits and networks, Electronic Components and Devices, Analog Electronics, Digital Electronics, Signals and Systems, Linear and Digital Control Theory.

Electromagnetic Waves, Probability and Random Processes, Communication Theory, Communication Circuits, Transmission Lines, Wave Guides, Antennas, Microwave devices and Circuits, Data Communications, Communication Networks, Satellite Communication, Optical Communication.

Time domain analysis of discrete-time systems - Basic discrete time signals, discrete-time Fourier Series, Z Transform – definition and properties, Discrete-time Fourier Series and its properties, Properties and applications of DTFT. Relationship between time, Z- and frequency domains, DFT fundamentals and Properties of DFT, FIR and IIR filters.

Algorithm analysis, Asymptotic notations. Divide and Conquer algorithms, Analysis of divide and conquer algorithms, sort and search algorithms, Data structures, Linked list, stacks, queues and graphs.

Linear and Digital ICs, Digital System Design, VLSI Technology, CMOS VLSI, Mixed Signal Design, HDL, Data converters, Microprocessors, Computer Architecture and organization, Logic Synthesis, DSP Architectures, Embedded Systems.

Weightage of different academic components for evaluation (As per the information brochure):

MTech (Research) and MTech (Sponsored)

UG (Academic performance in the qualifying examination)	10%
GATE	70%
Written Test	10%
Technical Presentation/ Interview (Research Aptitude/ Technical knowledge/ Subject Knowledge)	10%

T. Ramesh

Head of the Department

May 05, 2025

प्राध्यापक एवं विभागाध्यक्ष/PROF & HEAD
इ. एवं सी. विभाग / Department of E & C
एन.आई.टी.के. सूरत्कल/NITK Surathkal
मंगलूर / MANGALURU - 575 025

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA SURATHKAL
P.O. SRINIVASNAGAR, MANGALURU-575 025
Telephone: 0824-2473046, Website: www.ece.nitk.ac.in

Date: 05-05-2025

Shortlisted candidates for M Tech (Research / Sponsored) Programme–
Written Aptitude Test / Interview for the year 2025-26

With reference to your application for admission to M. Tech (Research / Sponsored) Programme in the department of Electronics and Communication Engineering, you are requested to appear for the Written test/Interview at NITK Surathkal. You should produce all the original records such as Date of Birth Certificate, GATE Score Card, Degree Certificate and Marks Cards of all semesters (UG programme), if result of the final year exam is awaited then provide a certificate from the head of your institution which states that you are the final year student of (branch) appearing / appeared for the final year / semester examination during academic year 2024-25 and results are awaited, SC/ST/OBC-NCL/EWS certificate (if applicable as per proforma), OBC-NCL / EWS certificate should be obtained from competent authority as specified in the NITK website and must be dated on or after April 1, 2025, Person with disability certificate (if applicable), Sponsorship letter (if applicable), Conduct Certificate and valid photo identity card. Please keep a self-attested photocopy of all these certificates readily available at the time of interview.

Department	Department of Electronics and Communication Engineering
Place of Reporting	Department of Electronics and Communication Engineering, NITK Surathkal
Document verification	May 21, 2025, 9:00AM onwards
Written Test Date and Time	May 21, 2025, 2:00PM at ECE Department
Announcement of shortlisted candidates for interview	May 21, 2025, 5:00 PM
Interview Date and Time	May 22, 2025, 9:00 AM Onwards, Meeting room, ECE Department

NOTE:

1. Candidates should be prepared to appear for a written Aptitude Test before the interview.
2. Fee Structure for M Tech (Sponsored/ Research) programme and Course syllabus are provided on Institute's website, i.e. www.nitk.ac.in. A copy of the syllabus for the aptitude test is given in a separate page.
3. Full-time/External Registrants - sponsored from Industry or other organizations, should have been serving in the sponsoring organisation for a period of **at least 2 years** after qualifying degree and have to produce a letter from their employer stating that the candidate is deputed for M. Tech/ M. Tech (Research) in the Institute on full salary during the study period. The employer should indicate that the candidate will not be withdrawn midway before the completion of the course. (Sponsorship letter should be in the format provided in the Application Form).
4. Candidates who have not submitted marks of final examination along with application form shall produce the same at the time of admission if available.
5. Your candidature for this test is provisional & is subject to your fulfilling the educational qualifications & other criteria prescribed for the programme as mentioned in the Information Brochure, failing which your candidature can be summarily rejected after verification/scrutiny at a later stage.
6. Please keep the Admit Card ready during the offline test and interview. You are responsible for safe custody of the Admit Card and in the event of any other person using this Admit Card, the responsibility lies on you to prove that you have not used the service of an impersonator.
7. Please note that no expenses shall be payable for appearing in the written test/Interview.

M Ramesh

Head of the Department

May 05, 2025

प्राध्यापक एवं विभागाध्यक्ष/Prof. & HEAD
इ. एवं सी. विभाग / Department of E & C
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